GALLIUM ARSENIDE IMPATT DIODES AT 20 GHZ*

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Abstract

High performance double-drift Read GaAs IMPATT diodes have yielded power levels of 4 W CW with 20 percent efficiency at 20 GHz with a junction temperature less than 250° C. In this paper we describe the profile, chip and thermal design of such diodes. It is shown that further improvements in thermal design should result in diodes giving up to 8 W CW.

Electrical series resistance and package parasitics are important parameters in determining the device performance and amplifier bandwidth. We show that there need not be a tradeoff between thermal and parasitic characteristics of a 20 GHz diode package.

Introduction

Gallium arsenide CW double-drift IMPATT diodes have demonstrated excellent performance at X-band (10 W, 21% efficiency) and at 35 GHz (3 W, 22% efficiency).[1] This paper describes our efforts to develop high power CW, 20 GHz diodes.

The key elements in achieving high power and efficiency are:

1. Development of a diode doping profile which permits a high ratio of rf voltage to operating dc voltage prior to negative conductance rolloff.

2. Development of a material and fabrication technology which results in the lowest possible value of parasitic series resistance.

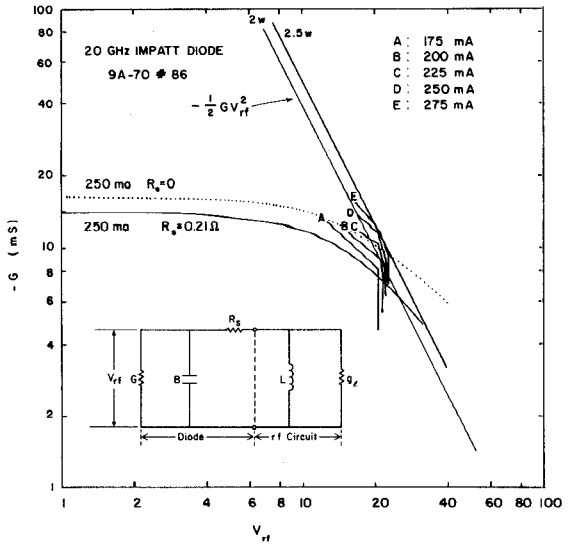

Fig. 1 Comparison between measured and calculated diode conductance. C_d = 1 pF. The inset shows an equivalent circuit.

3. Development of a chip and package design which will result in the lowest possible value of thermal resistance.

Instantaneous bandwidths up to 5 percent are often necessary in communications applications. This puts additional requirements on the package parasitics and tuning elements used.

Our ongoing research program addresses each of these points. We have so far demonstrated chip level power output of 4 W CW for diodes on copper heatsinks at an efficiency of 20 percent. It will be shown that improved heatsink technology can result in increasing the power output levels up to 8 W CW.

Diode Conductance

Figure 1 shows an equivalent circuit representation of the diode and its rf circuit referred to the chip. For a given doping profile, the negative conductance (G) is a function of the dc bias current and the rf terminal voltage, V_{rf}. This is shown by the data of Fig. 1. The curves with associated values of parasitic series resistance, R_s, have been calculated by an analytical model.[1] The curves A through E have been measured using the device in an oscillator circuit whose impedance has been determined separately.

It can be seen that $|G|$ falls abruptly at a limiting value of V_{rf}. This appears to be a characteristic of diodes at all frequency ranges so far studied and is not predicted by the analytical theory. Since the high power operating points are along the contours tangent to the conductance knee, it is the objective of our profile development to extend the knee to the highest possible value of V_{rf}. The ratio of V_{rf} to the dc bias voltage (modulation ratio) determines the diode efficiency. Speculation on the cause of the conductance rolloff centers on the occurrence of drift zone avalanche at the high end of the rf voltage swing or carrier velocity desaturation at the low end. Our profile design goals are aimed at empirically optimizing

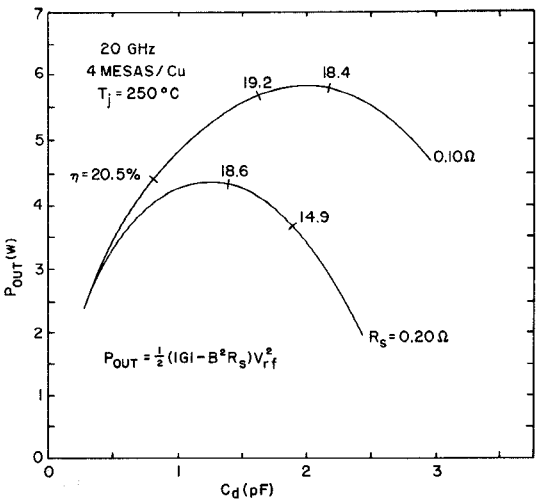

Fig. 2 Power output vs. junction capacitance.

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the electric field distribution to minimize these effects. The profiles used in our studies are double low-high-low double punchthrough structures with each drift zone thickness ∿ 0.8 microns and avalanche zone width ∿ 0.3 microns.

Electrical and Thermal Resistance

Excess series resistance can severely reduce the diode efficiency even for diodes with a high modulation ratio. This results because the circulating reactive current, $B \cdot V_{rf}$, must flow through R_s producing a power loss $(\frac{1}{2})R_s(B \cdot V_{rf})^2$. Since $B \cong 2\pi f C_d$ with C_d, the diode capacitance, the effect becomes more severe in large area, high junction capacitance devices for a given R_s. This is illustrated in Fig. 2 where output power vs. junction capacitance is calculated at a junction temperature of 250° C for a modulation ratio of 0.5 and different values of R_s. Since R_s can be measured separately[2] the modulation ratio for each profile can be calculated from measured efficiency.

The thermal resistance θ is a function of junction capacitance, $\theta \alpha C_d^{-1/2}$. Hence, as the junction capacitance increases from zero, the dissipated (and input) power can increase and so does the power output. In the case $R_s = 0$ the power output would continue to increase monotonically. However, for $R_s \neq 0$ the effects mentioned above cause the power to fall for large C_d. The result is an optimum capacitance as shown in the figure. Note that higher efficiencies are achieved below the optimum capacitance.

For a given junction temperature, the value of thermal resistance at the optimum capacitance determines the maximum output power. There is thus an intimate relationship between optimum junction capacitance, and electrical and thermal resistance. This is shown in Fig. 3. The capacitance for maximum power is plotted for four thermal designs under study. At a junction capacitance of 1.3 pF the four designs give the following thermal resistances: single mesa diode/copper heatsink (14 °C/W); 4 mesa diode/copper heatsink (11 °C/W); single mesa diode/diamond heatsink (9 °C/W); 4 meas diode/diamond heatsink (6 °C/W).

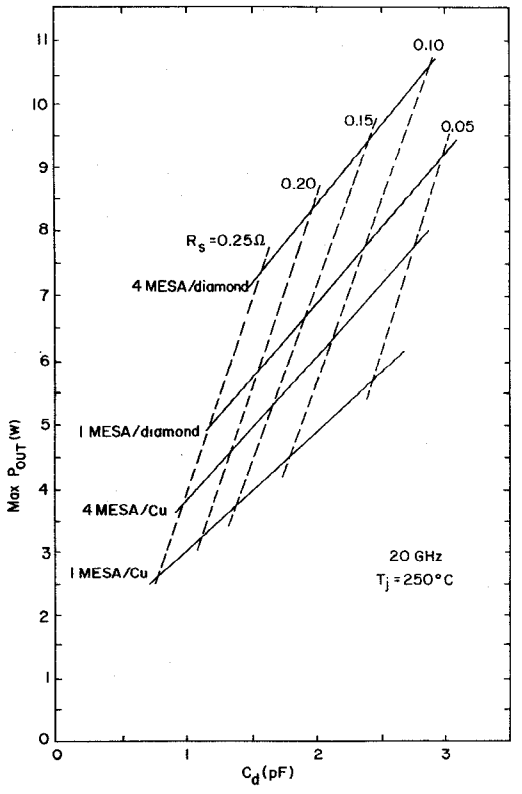


Fig. 3 Design contours for junction capacitance at maximum power output. Device geometry and series resistance are parameters. Circuit tuning could be difficult for $C_d > 2$ pF.

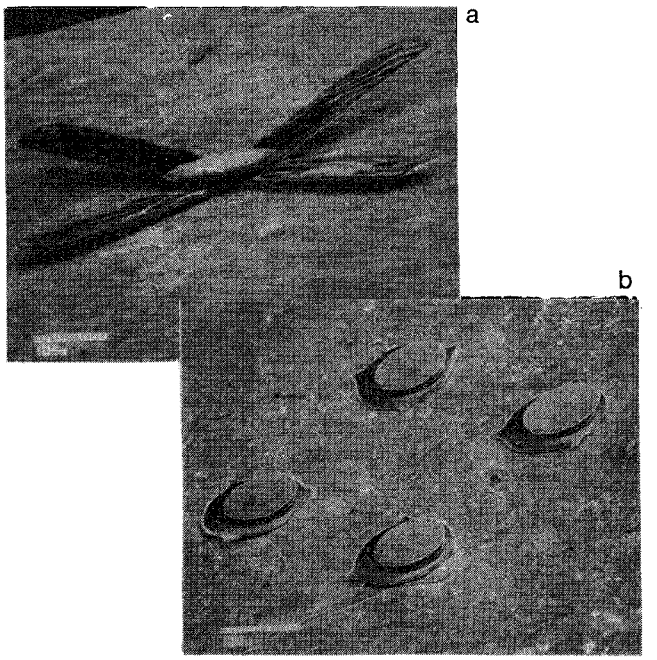


Fig. 4 Electron micrographs of chips used in our studies. (a) The single mesa diameter is approximately 0.006 in.; (b) Each of the four mesas is approximately 0.003 in. diameter.

The 4 mesa diode on diamond heatsink is presently under development. The thermal resistances quoted for the other three designs have already been achieved in our laboratory. Scanning electron micrographs of the single mesa beam lead and 4-mesa diodes are shown in Fig. 4. In the 4 mesa case the mesas are connected in parallel by a bonded wire mesh.

The advantages of 4 mesa[3] chips and diamond heatsinks[4] are evident in Fig. 3. The lower thermal resistances permit larger area diodes since the associated higher bias currents increase G relative to B^2R_s. For realistic values of $R_s \cong 0.15$ ohms, it can be seen that 9 W CW can be obtained from the 4 mesa diamond heatsink chip. This estimate must be tempered somewhat by circuit tuning limitations since it might prove difficult to match a 20 GHz diode with $C_d > 2$ pF. At 1.3 pF the power output would be about 8 W at T_j = 250° C with 19 percent conversion

TABLE I
20 GHZ DIODE PERFORMANCE

Diode	Geometry	Measured R_s (a) (ohm)	θ (b) (°C/W)	P_{out} (c) (W)	T_j (d) (°C)	η (%)	Calculated V_{rf}/V_{dc}
9A-98-F30	QUAD/Cu H.S.	0.19	14.0	4.0	332	21	0.61
9A-70-86	QUAD/Cu H.S.	0.23	19.7	2.3	218	19	0.60
9E-36-3	S.M/Cu H.S.	0.13	13.2	3.2	263	15	0.38
9E-39-3	S.M/Cu H.S.	0.14	17.2	1.9	244	13	0.39
9E-39-75	S.M/Cu H.S.	0.11	9.7	3.5	267	12	0.34

(a) Threshold method (Ref. 2)
(b) Junction areas vary
(c) At the reference plane of the chip
(d) Pedestal temperature = 25° C

efficiency. We have again assumed a modulation ratio of 0.5.

The performance levels achieved to date in a Kurokawa circuit[5] are summarized in Table I. Power levels quoted are corrected to account for the measured circuit efficiency (∿ 70%). Circuit efficiency is defined as the ratio of the power delivered to the external load to the power at the reference plane of the diode chip. The 9E diode profile had lower series resistances but had modulation ratios below 0.4. The 9A profiles had higher values of R_S but modulation ratios ∿ 0.6. Enough circuit tuning conditions were tried that we are reasonably sure that the different modulation ratios were due to doping profile rather than circuit tuning.

Package Parasitics and Amplifier Bandwidth

As noted in the Introduction, IMPATT diode communications amplifiers can require bandwidths up to 5 percent. This requirement could dictate a restriction on the package used if excess parasitic reactances prove to be bandwidth limiting tuning elements. It was considered that in the ceramic package designs of Fig. 5, the 4 mesa diode with 0.025 in. center to center mesa spacing requires a ceramic inside diameter of 0.050 in. while for the single mesa chip this can be reduced to 0.014 in. If the parasitics associated with the large package were too great, diodes of the lowest thermal resistance could not be used in a broadband amplifier. To test for this limitation each of the two packages and circuit mount parasitics in a Kurokawa test circuit[5] were represented by a double L-network. The lumped elements were determined by curve fitting broadband S-parameter measurements using known transformers. The results are shown in Table II.

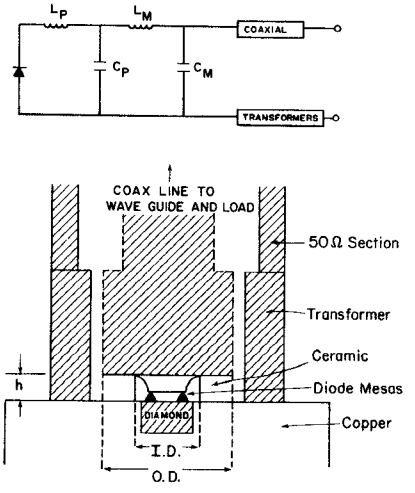


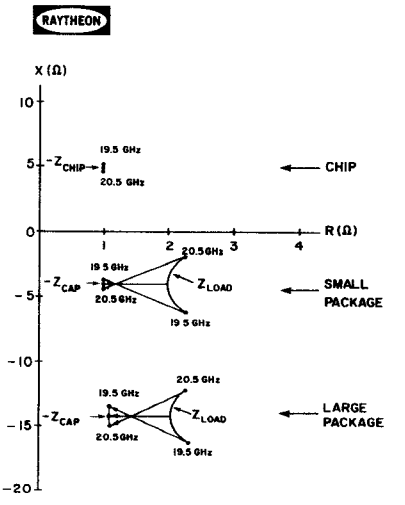
Fig. 5 Equivalent circuit and mechanical drawing of a packaged diode in a waveguide mount.

The effects of these parasitic reactances on amplifier bandwidth can be seen from the impedance loci[6]

TABLE II
PACKAGE CHARACTERISTICS

Package Type	OD	ID	h	C_m	L_m	C_p	L_p
	(milli inches)			(pF)	(nH)	(pF)	(nH)
Large (11)	80	50	20	.07	.11	.44	.03
Small (EHF)	30	14	6	.09	.05	.14	.02

* See Fig. 5 for definitions



COMPARISON OF THE EFFECT OF PACKAGE PARASITICS ON BANDWIDTH FOR THE SMALL AND LARGE PACKAGES

Fig. 6 Impedance loci for chip and circuit at the reference plane of the diode cap for the two packages under study.

at the reference plane of the diode cap as seen in Fig. 6. The gain is inversely proportional to the vactor separation of the diode and measured circuit locus. For both the large and small packages, the frequency dispersion in this data is dominated by the Kurokawa cavity resonance and not the dispersion due to the package parasitics. Indeed, much of the dispersion in the diode characteristic is due to the chip capacitance itself. It is concluded that there need not be a tradeoff between amplifier bandwidth and thermal design.

Acknowledgement

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References

1. M. G. Adlerstein and E. L. Moore, "Microwave properties of GaAs IMPATT diodes at 33 GHz," Proc. Eighth Biennial Cornell Electrical Engineering Conference (Aug. 1981).

2. M. G. Adlerstein, L. H. Holway, and G. Chu, "Measurement of series resistance in IMPATT diodes," to be published IEEE Trans. Elec. Devices (1982).

3. J. Frey, "Multimesa vs. annular construction for high average power in semiconductor devices," IEEE Trans. on Electron Devices ED-19 (1972), p. 981.

4. R. Berman, "Physical properties of diamond," (1965), Clarendon Press, Oxford.

5. K. Kurokawa and F. M. Magolhaer, "An X-band 10 W multiple IMPATT oscillator," Proc. IEEE 59, 102 (1971).

6. K. Kurkowa, "Injection locking of microwave solid-state oscillators," IEEE Proc. 61, 10, pp. 1386-1410 (1973).